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| 10/573,775 | 03/28/2006 | Shunpei Yamazaki | 740756-2941 | 5479 |

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| EXAMINER | |
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| STAHL, MICHAEL J | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/573,775 | YAMAZAKI ET AL. | |
| | Examiner | Art Unit | |
| | MICHAEL STAHL | 2874 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *27 November 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-66* is/are pending in the application.

4a) Of the above claim(s) *1-20 and 22-66* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 March 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/21/08,3/28/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

### *Election*

Applicant's election without traverse of claim 21 in the reply filed on 11/27/2009 is acknowledged. Claims 1-20 and 22-66 are withdrawn from further consideration pursuant to 37 CFR 1.142(b).

### *Specification*

The specification is objected to for containing the following minor errors:

At p. 18, line 1, "101" should be inserted after "base film". See fig. 1A.

At p. 21, line 28, "visocosity" should be changed to "viscosity".

At p. 23, line 12, "insulting" should be changed to "insulating".

### *Claim Rejections - 35 USC § 103*

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Koh et al. (US 5427976) in view of Hashimoto et al. (US 2003/0083203, cited in information disclosure statement).

First Interpretation: Koh discloses a method for manufacturing a TFT, comprising the steps of: forming a first insulating film **42** having a depression (the etched trench) and a projection (the higher surfaces outside of the trench); forming a conductive film **43** (p-type polysilicon, which acts as a gate electrode) in the depression; forming a second insulating film **45** so as to cover the first insulating film and the conductive film; forming a semiconductor film **47** (high concentration impurity layer) over the second insulating film (fig. 15); and simultaneously patterning the second insulating film and the semiconductor film (fig. 16), wherein the first insulating film and the conductive film are formed so that the surfaces thereof are flat. See col. 7 lns. 21-49. In this interpretation, the monocrystalline silicon layer **45** is taken as an insulating film at least since its conductivity is lower than that of layer **47**. It is noted that "conductive", "semiconductive", and "insulating" are relative terms; for example water can conduct electricity but not nearly as well as silver.

Second Interpretation: Koh discloses a method for manufacturing a TFT, comprising the steps of: forming a first insulating film **42** having a depression (the etched trench) and a projection (the higher surfaces outside of the trench); forming a conductive film **43** (p-type polysilicon, which acts as a gate electrode) in the depression; forming a second insulating film **46** (oxide layer) so as to cover the first insulating film and the conductive film; forming a semiconductor film **45** (monocrystalline silicon) over the second insulating film (fig. 15); and

simultaneously patterning the second insulating film and the semiconductor film (fig. 16), wherein the first insulating film and the conductive film are formed so that the surfaces thereof are flat. See col. 7 lns. 21-49. In this interpretation, "over" in line 8 of claim 21 is broadly interpreted as "spanning" and not as strictly limited to being on the side of the second insulating film which is farther from the first insulating film.

In either interpretation above, Koh does not specifically disclose that the conductive film is formed in the depression by spurting droplets containing a conductive material. Koh appears to use a chemical vapor deposition process to form the polysilicon material of the gate electrode (col. 4 lns. 55-65). Hashimoto teaches that CVD of polysilicon has certain disadvantages, such as susceptibility to contamination, low film formation speed, expensive equipment, and generation of excessive waste material ([0019]-[0025]). The alternative deposition process proposed by Hashimoto involves spurting droplets of a solution containing the material to be deposited ([0032]), which may include silicon ([0059]); also see the embodiment described at [0162]-[0189]. A skilled person could have used the Hashimoto process to deposit the polysilicon **43** in the trench of the Koh device, and the results would have been predictable. Accordingly it would have been obvious to a skilled person at the time the invention was made to do so, motivated by the expectation of avoiding the disadvantages of CVD mentioned by Hashimoto.

It is noted that in Koh a boron diffusion process is used to dope the polysilicon film **3** (see col. 4 lns. 55-65), presumably to make it even more conductive. However, it is asserted that the silicon in the inkjetted solution (using the Hashimoto method) is itself fairly regarded as a conductive material by reasoning similar to what was stated above in the "First Interpretation".

In other words, silicon is typically more electrically conductive than silicon dioxide (film **42** in Koh).

Claims 23-25 and 27 are currently written as alternatively dependent from claims 20-22 (with claim 26 depending from claim 25). Claims 31 and 34 are currently written as alternatively dependent from claims 20-22 and 28-30. In the event that claims 23-25, 27, 31, and 34 are rewritten to depend solely from claim 21, it appears that they would be unpatentable over Koh in view of Hashimoto. For example, Hashimoto discloses that insulating materials can also be deposited by spurting droplets ([0059]), **44** or **46** in Koh is an insulating film over a channel region of the semiconductor film, and the dimensions of the depression or the amount of droplets to be spurted are engineering choices which depend on the particular design of a device to be manufactured.

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Roy (US 6180976) in view of Drummond et al. (US 5132248, cited in information disclosure statement).

Roy discloses a method for manufacturing a TFT, comprising the steps of: forming a first insulating film **18** having a depression **30** and a projection (e.g. region between **30** and **32**) (fig. 2); forming a conductive film **12** (fig. 4; it is derived from film **38** in fig. 3) in the depression; forming a second insulating film **14** so as to cover the first insulating film and the conductive film (fig. 5); forming a semiconductor film **42** (**42** is called a conductive material at col. 8 lns. 14-15, but note that semiconductors such as doped silicon or polysilicon are included in the class of conductive materials as mentioned at col. 1 lns. 32-33) over the second insulating film (also fig. 5); and simultaneously patterning the second insulating film and the semiconductor film (fig.

6), wherein the first insulating film and the conductive film are formed so that the surfaces thereof are flat. It is acknowledged that the Roy device is not a thin film transistor; however, "thin film transistor" as recited in the preamble is merely a label for the manufactured device in this context since it does not define any structure of the device.

Roy does not specifically disclose that the conductive film is formed in the depression by spurting droplets containing a conductive material. It is noted however that the conductive film is initially applied over the whole substrate as a layer **38**, much of which is later removed by a chemical-mechanical polishing (CMP) process to form the desired conductive film **12** (see figs. 3-4). Drummond teaches that a conductive pattern can be deposited by spurting (inkjetting) droplets containing a conductive material; see e.g. col. 3 lns. 52-62, col. 4 lns. 47-51, and so forth. A skilled person could have used the inkjet process taught by Drummond to directly deposit the conductive film **12** into the groove **30** in the Roy device, and the results would have been predictable. Accordingly it would have been obvious to a skilled person at the time the invention was made to do so, motivated by the expectation of reduced material usage and/or waste. In particular, the inkjet process of Drummond enables deposition at a precise location, so that it is not necessary to use extra conductive material to coat the whole substrate and then etch or polish it back as in the original Roy process. It is also noted that the proposed combination does not preclude subsequently using CMP to planarize the surface **40** as mentioned at col. 7 lns. 47-50; it merely reduces the overall amount of conductive material required.

***Conclusion***

US 2003/0059987 discloses inkjet printing of integrated circuits. US 2006/0176413 discloses a relevant TFT fabrication method but does not qualify as prior art.

Inquiries about this letter may be directed to examiner Stahl at 571-272-2360. Inquiries of a general or clerical nature (e.g., a request for a missing form or paper, etc.) should be directed to the technical support staff supervisor at 571-272-1626. Official correspondence which is eligible for submission by facsimile and which pertains to this application may be faxed to 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Questions about the Private PAIR system should be directed to the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Mike Stahl/
Primary Examiner, Art Unit 2874

February 7, 2010